Amendments to the Specification:

Please delete the [0037] on page 10 of the application and insert in place thereof the following rewritten paragraph:

[0037]   Independent of introducing the abbreviated timing delay to the simulated synchronous sequence 44, step 58 of Fig. 1 introduces an extended timing delay of the system environment to generate a second simulated synchronous sequence of states. In one embodiment, the extended delay is the estimated worst case, or a maximum timing delay, of the system environment, excluding any delay associated with the chip or the tester. However, there may be [[am]] an error tolerance adjustment. Fig. 2B shows a simulated synchronous extended-delay sequence 60 having a timing delay 62 of 10 ns. By introducing the timing delay, each cycle 46 of the simulated synchronous sequence 44 of Fig. 2A is shifted along the time domain by 10 ns, resulting in the simulated synchronous extended-delay sequence 60. The simulated synchronous extended-delay sequence includes repeating shifted cycles 64.

Please delete paragraph [0050], beginning on page 14 and continuing on page 15 of the application, and insert in place thereof the following rewritten paragraph:

[0050]   Each overlapping cycle 140 of the synchronous sequence 138 of test vectors includes a time interval at which an output state can be properly sampled by the tester. Fig. 6 shows an expanded view of the overlapping cycle 140 of Fig. 5 within the base period 126. A sampling instance 144 is fixed at a timing location within a timing interval 142 of the cycle. The location of the sampling instance should correspond to a rising clock edge [[20]] 149 of the tester cycle 18 (Fig. 2A). The placement of the sampling instance should include a sufficient time interval 146 (i.e., T_{setup}) before the sampling instance and a sufficient time interval 148 (i.e., T_{hold}) after the sampling instance, but within the timing interval, to ensure an adequate sampling of data by the tester. The selection of the location of the sampling instance is repeated in every tester period such that the output data of the synchronous sequence of test vectors will be sampled at substantially identical times and locations in successive tester periods.